

Achronix Joins TSMC IP Alliance Program



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SANTA CLARA, Calif., Sept. 25, 2019 /PRNewswire/ -- [Achronix Semiconductor Corporation](#), a leading provider in FPGA-based hardware accelerator devices and high-performance eFPGA IP, has joined the TSMC IP Alliance Program, a key component of TSMC Open Innovation Platform® (OIP). Achronix's award-winning Speedcore™ eFPGA IP is optimized for high-end and high-performance applications. Speedcore eFPGA IP is available today on TSMC 16nm FinFET Plus (16FF+) and N7 process technologies, and it will be soon available on TSMC 12nm FinFET Compact Technology (12FFC).

Achronix previously announced its Gen4 FPGA architecture for Speedcore IP, which is available to use today. Compared to the previous Speedcore architecture, the Speedcore Gen4 architecture increases performance by 60%, reduces power by 50% and die area by 65%, while retaining the original abilities of Speedcore eFPGA IP to bring programmable hardware acceleration capabilities to a broad range of high-performance computing, networking and storage applications. Achronix will demonstrate how its Speedcore eFPGA IP is uniquely sized and optimized for each customer's application in its booth (#420) at TSMC Open Innovation Platform® Ecosystem Forum in Santa Clara on September 26.

"Achronix Speedcore eFPGA IP delivers the optimal balance of highest-performance hardware acceleration functionality while retaining the flexibility to adapt for new workloads. This is a critical design requirement for SoCs development in compute, networking and storage offload," said Steve Mensor, vice president, marketing at Achronix. "Achronix is the only company that offers both high-performance standalone FPGA-based data accelerators and eFPGA IP technology. Companies interested in using Achronix Speedcore eFPGA for their ASIC/SoC can be confident that they are getting the same high-quality FPGA technology that Achronix uses in its own products."

Speedcore eFPGA IP is a fully scalable architecture supporting sizes from 5K 6-input look-up-tables (6LUTs) to 1M 6LUTs along with other programmable blocks including memories, DSP blocks for filtering and MLP blocks optimized for AI/ML. Speedcore IP is supported by Achronix's high-quality ACE design tools.

"CPU Core, GPU Core, and now eFPGA are critical IP for silicon innovations focusing on the rapidly changing applications in the areas including artificial intelligence, 5G wireless infrastructure, automotive and edge computing," said Suk Lee, TSMC Senior Director, Design Infrastructure Management Division. "We're glad to see Achronix joining our IP Alliance Program with its optimized Speedcore eFPGA IP solution, enabling our customers to achieve a smooth design experience, ease of design reuse and fast integration into the overall design system."

About Achronix Semiconductor Corporation

Achronix Semiconductor Corporation is a privately held, fabless semiconductor corporation based in Santa Clara, California and offers high-performance FPGA and embedded FPGA (eFPGA) solutions. Achronix offerings include programmable FPGA fabrics, discrete high-performance and high-density FPGAs with hardwired system-level blocks, datacenter and HPC hardware accelerator boards, and best-in-class EDA software supporting all Achronix products. The company has sales offices and

representatives in the United States, Europe, and China, and has a research and design office in Bangalore, India.

Find out more at <https://www.achronix.com>.

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